THE INVENTION CLAIMED IS:

1. A method for selectively depositing silicon oxide onto a silicon-comprising substrate, the method comprising the steps of:

providing the silicon-comprising substrate having exposed regions of different type conductivity; and

reacting ozone and tetraethylorthosilicate in contact with the substrate to selectively deposit silicon oxide onto the substrate, whereby, compared to exposed regions of non-doped silicon, the silicon oxide deposits at a faster rate on exposed regions of P-type silicon and at a slower rate on exposed regions of N-type silicon.

2. A method for selectively depositing silicon oxide onto a silicon-comprising substrate, the method comprising the steps of:

providing the silicon-comprising substrate having exposed regions of different type conductivity; and

reacting ozone and tetraethylorthosilicate in contact with the substrate to selectively deposit silicon oxide onto the substrate, whereby, compared to

exposed regions of non-doped silicon, the silicon oxide deposits at a faster rate on exposed regions of P-type silicon and at a slower rate on exposed regions of N-type silicon, wherein the reaction occurs at a temperature up to about 500° C and a pressure of at least about 10 torr.

3. The method of Claim 2, wherein the reaction occurs at a temperature up to about 400° C.

4. The method of Claim 2, wherein the reaction occurs at a pressure of at least about 300 torr.

5. A semiconductor processing method of forming spacers of variable thickness, the method comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first conductive region comprising either P-type silicon or non-doped silicon and at least one second conductive region, provided that:

(1) when the first conductive region comprises P-type silicon, then the second conductive region comprises either non-doped silicon or N-type silicon; and,

(2) when the first conductive region comprises non-doped silicon, then the second conductive region comprises N-type silicon;

depositing silicon oxide, in a single process step, to form a layer over the silicon-comprising substrate and both the first conductive region and the second conductive region, whereby a greater thickness of silicon oxide is deposited on the first conductive region than on the second conductive region; and

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the first and second conductive regions provides a layer of variable thickness around the first conductive region and the second conductive region.

6. A semiconductor processing method of forming spacers of variable thickness, the method comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first conductive region comprising either P-type silicon or non-doped silicon and at least one second conductive region, provided that:

(1) when the first conductive region comprises P-type silicon, then the second conductive region comprises either non-doped silicon or N-type silicon; and,

(2) when the first conductive region comprises non-doped silicon, then the second conductive region comprises N-type silicon;

decomposing tetraethylorthosilicate with ozone to selectively deposit silicon oxide over the silicon surface and over both the first conductive region and the second conductive region, whereby a greater thickness of silicon oxide is deposited on the first conductive region than on the second conductive region; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the first and second conductive regions provides a layer of variable thickness around the first conductive region and the second conductive region.

7. A semiconductor processing method of forming spacers of variable thickness, the process comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first conductive region comprising either P-type silicon or non-doped silicon and at least one second conductive region, provided that:

(1) when the first conductive region comprises P-type silicon, then the second conductive region comprises either non-doped silicon or N-type silicon; and,

(2) when the first conductive region comprises non-doped silicon, then the second conductive region comprises N-type silicon;

contacting silicon-comprising substrate with ozone and tetraethylorthosilicate whereby the first conductive region and the second conductive region are in intimate contact with the ozone and the tetraethylorthosilicate;

reacting the ozone and the tetraethylorthosilicate at a temperature up to about 500° C and a pressure of at least about 10 torr to selectively deposit silicon oxide over the substrate surface and both the first conductive region and the second conductive region, whereby a greater thickness of silicon oxide is deposited on the first conductive region than on the second conductive region; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the first and second conductive regions provides a layer of variable thickness around the first conductive region and the second conductive region.

8. The method of Claim 7, wherein the reaction occurs at a temperature up to about 400°C.

9. The method of Claim 7, wherein the reaction occurs at a pressure of at least about 300 torr.

10. A semiconductor processing method of forming spacers of variable thickness, the method comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first protrusion comprising either P-type silicon or non-doped silicon and at least one second protrusion, provided that:

(1) when the first protrusion comprises P-type silicon, then the second protrusion comprises either non-doped silicon or N-type silicon; and,

(2) when the first protrusion comprises non-doped silicon, then the second protrusion comprises N-type silicon;

depositing silicon oxide, in a single process step, over the wafer surface and both the first protrusion and the second protrusion, whereby a greater thickness of silicon oxide is deposited on the first protrusion than on the second protrusion; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the first and second protrusions provides a layer of variable thickness around the first protrusion and the second protrusion.

11. A semiconductor processing method of forming spacers of variable thickness, the method comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first protrusion comprising either P-type silicon or non-doped silicon and at least one second protrusion, provided that:

(1) when the first protrusion comprises P-type silicon, then the second protrusion comprises either non-doped silicon or N-type silicon; and,

(2) when the first protrusion comprises non-doped silicon, then the second protrusion comprises N-type silicon;

decomposing tetraethylorthosilicate with ozone to selectively deposit silicon oxide over the silicon surface and both the first protrusion and the second protrusion, whereby a greater thickness of silicon oxide is deposited on the first protrusion than on the second protrusion; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the first and second protrusions provides a layer of variable thickness around the first protrusion and the second protrusion.

12. A semiconductor processing method of forming spacers of variable thickness, the method comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first protrusion comprising either P-type silicon or non-doped silicon and at least one second protrusion, provided that:

(1) when the first protrusion comprises P-type silicon then the second protrusion comprises either non-doped silicon or N-type silicon; and,

(2) when the first protrusion comprises non-doped silicon then the second protrusion comprises N-type silicon;

contacting the wafer surface with ozone and tetraethylorthosilicate whereby the first protrusion and the second protrusion are in intimate contact with the ozone and the tetraethylorthosilicate;

decomposing the tetraethylorthosilicate with the ozone to selectively deposit silicon oxide over the wafer surface and both the first protrusion and the second protrusion, whereby a greater thickness of silicon oxide is deposited on the first protrusion than on the second protrusion; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers

remaining on the first and second protrusions provides a layer of variable thickness around the first protrusion and the second protrusion.

13. A semiconductor processing method of forming spacers of variable thickness, the process comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first protrusion comprising either P-type silicon or non-doped silicon and at least one second protrusion, provided that:

(1) when the first protrusion comprises P-type silicon, then the second protrusion comprises either non-doped silicon or N-type silicon; and,

(2) when the first protrusion comprises non-doped silicon, then the second protrusion comprises N-type silicon;

reacting ozone and the TEOS at a temperature up to about 500° C and a pressure of at least about 10 torr to selectively deposit silicon oxide over the wafer surface and both the first protrusion and the second protrusion, whereby a greater thickness of silicon oxide is deposited on the first protrusion than on the second protrusion; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the

first and second protrusions provides a layer of variable thickness around the first protrusion and the second protrusion.

14. The method of Claim 13, wherein the reaction occurs at a temperature up to about 400°C.

15. The method of Claim 13, wherein the reaction occurs at a pressure of at least about 300 torr.

16. A semiconductor processing method of forming wordlines with spacers of variable thickness, the process comprising the steps of:

providing a silicon comprising substrate having a surface comprising at least one first wordline comprising P-type silicon and at least one second wordline comprising N-type silicon, the first and second wordlines being separated on the substrate;

contacting the substrate with ozone and tetraethylorthosilicate whereby the first wordline and the second wordline are in intimate contact with the ozone and the tetraethylorthosilicate;

reacting the ozone and the tetraethylorthosilicate to selectively deposit silicon oxide over the substrate surface and both the first wordline and the second

wordline, whereby a greater thickness of silicon oxide is deposited on the first wordline than on the second wordline; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the first and second wordlines provides a layer of variable thickness around the first wordline and the second wordline.

17. A semiconductor processing method of forming wordlines with spacers of variable thickness, the process comprising the steps of:

providing a silicon-comprising substrate having a surface comprising at least one first wordline comprising P-type silicon and at least one second wordline comprising N-type silicon:

reacting ozone and tetraethylorthosilicate at a temperature up to about 500° C and a pressure of at least about 10 torr to selectively deposit silicon oxide over the wafer surface and both the first wordline and the second wordline, whereby a greater thickness of silicon oxide is deposited on the first wordline than on the second wordline; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers

remaining on the first and second wordlines provides a layer of variable thickness around the first wordline and the second wordline.

18. The method of Claim 11, wherein the reaction occurs at a temperature up to about 400°C.

19. The method of Claim 11, wherein the reaction occurs at a pressure of at least about 300 torr.

20. A semiconductor processing method of forming dual gate structures with spacers of variable thickness, the process comprising the steps of:

providing a silicon comprising substrate having a surface comprising at least one first gate comprising P-type silicon and at least one second gate comprising N-type silicon:

contacting the substrate with ozone and tetraethylorthosilicate whereby the first gate and the second gate are in intimate contact with the ozone and the tetraethylorthosilicate;

reacting the ozone and the tetraethylorthosilicate to selectively deposit silicon oxide over the substrate surface and both the first gate and the second gate,

whereby a greater thickness of silicon oxide is deposited on the first gate than on the second gate; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers remaining on the first and second gates provides a layer of variable thickness around the first gate and the second gate.

21. A semiconductor processing method of forming dual gate structures with spacers of variable thickness, the process comprising the steps of:

providing a silicon comprising substrate having a surface comprising at least one first gate comprising P-type silicon and at least one second gate comprising N-type silicon:

reacting ozone and tetraethylorthosilicate at a temperature up to about 500°C and a pressure of at least about 10 torr to selectively deposit silicon oxide over the wafer surface and both the first gate and the second gate, whereby a greater thickness of silicon oxide is deposited on the first gate than on the second gate; and,

etching the silicon oxide deposited on the substrate to remove silicon oxide from the surface of the substrate, whereby the silicon oxide layers

remaining on the first and second gates provides a layer of variable thickness around the first gate and the second gate.

22. The method of Claim 21, wherein the reaction occurs at a temperature up to about 400°C.

23. The method of Claim 21, wherein the reaction occurs at a pressure of at least about 300 torr.

24. A semiconductor memory device comprising:

at least one first wordline comprising P-type silicon or polysilicon and a first nonconductive silicon oxide layer;

at least one second wordline comprising N-type silicon or polysilicon and a second nonconductive silicon layer; and

wherein the first layer is thicker than the second layer.

25. The semiconductor memory device of Claim 25, wherein the first and second spacers are formed using tetraethylorthosilicate/ ozone deposition in a one step process.

26. The semiconductor memory device of Claim 25, wherein at least one of the first wordline or the second wordline form part of a DRAM array.

27. The semiconductor memory device of Claim 25 wherein the DRAM array is part of a system-on-chip.

28. The semiconductor memory device of Claim 25, wherein at least one of the first wordline or the second wordline form part of an SRAM array.

29. The semiconductor memory device of Claim 25 wherein the SRAM array is part of a system-on-chip.

30. A multi-gate semiconductor device comprising:

at least one first P-type gate surrounded by a first nonconductive silicon oxide layer; and

at least one second N-type silicon gate surrounded by a second nonconductive silicon oxide layer;

wherein the first nonconductive spacer is thicker than the second nonconductive layer.

31. The multi-gate semiconductor device of Claim 30, wherein the device is part of a logic circuit.

32. The multi-gate semiconductor device of Claim 30, wherein the logic circuit is part of a system-on-chip.

33. A method for forming an oxide layer of varying thickness on a silicon-comprising substrate, comprising the steps of:

providing the silicon-comprising substrate having a surface and comprising at least a first region and a second region of different type conductivities; and

depositing silicon oxide onto the substrate in a single process step, to form an oxide layer over the first and second conductivity regions; whereby the oxide layer overlying the second conductivity region is thicker than the oxide layer overlying the first conductivity region.

34. The method of Claim 33, wherein each of the first and second regions comprise a structure formed on the surface of the substrate, with a portion of the substrate intermediate the structures having the oxide layer deposited thereon; and

the method further comprises the step of removing the oxide layer overlying the substrate between the first and second structures to expose the surface of the substrate.

35. The method of Claim 34, wherein the first and second structures comprise a silicon-comprising layer of a P-type or N-type conductivity, and an overlying salicide layer;

whereby, when the silicon-comprising layer of the first structure comprises a P-type conductivity, the silicon-comprising layer of the second structure comprises an N-type conductivity; and when the silicon-comprising layer of the first structure comprises an N-type conductivity, the silicon-comprising layer of the second structure comprises a P-type conductivity.